AMENDMENTS TO THE CLAIMS

Please replace all prior versions of the claims with the following claim listing:

Claims:

1-7. (Canceled)

8. (Currently Amended) A method of matching data and clock signal delays within receive logic, comprising the steps of:

minimizing setup and hold times of said receive logic;

formulating at least one miniaturized version of a clock buffer located within said receive logic, wherein said at least one miniaturized version of said clock buffer is a scaled down version of said clock buffer, said miniaturized version of said clock buffer having a scaling factor of K, said scaling factor representing a number of said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer; and

minimizing negative variations experienced by said clock buffer.

9. (Original) The method of claim 8, wherein said receive logic is situated on an application specific integrated circuit.

10. (Original) The method of claim 8, wherein said negative variations are selected from the group consisting of process, voltage and temperature.

11. (Original) The method of claim 8, wherein said clock buffer is capable of driving a received clock signal to a register located within said receive logic.

12. (Previously Presented) The method of claim 11, wherein a setup time of said receive logic is represented by the equation:

$$T_{setup} = T_{reg\text{-}setup} + 1.1 \times (-T_{clk\text{-}dly}) - T_{clk\text{-}rte}(min)$$

wherein, $T_{reg\text{-}setup}$ is a setup time for said register, $T_{clk\text{-}dly}$ is a delay contributed by said clock buffer, and $T_{clk\text{-}rte}(min)$ is a minimum delay contributed by propagation of said clock signal to said register.

13. (Previously Presented) The method of claim 11, wherein a hold time of said receive logic is represented by the equation:

$$T_{hold} = T_{reg\text{-}hold} + 1.1 \times (T_{clk\text{-}dly}) + T_{clk\text{-}rte}(max)$$

wherein, $T_{reg\text{-}hold}$ is a hold time for said register, $T_{clk\text{-}dly}$ is a delay contributed by said clock buffer, and $T_{clk\text{-}rte}(max)$ is a maximum delay contributed by propagation of said clock signal to said register.

14. (Original) The method of claim 8, wherein said clock buffer provides an amount of delay that slows progression of said clock signal in a path to a register located within said receive logic.

15. (Currently Amended) A system for matching data and clock signal delays within receive logic, comprising:

means for minimizing setup and hold times of said receive logic;

means for formulating at least one miniaturized version of a clock buffer located within said receive logic, wherein said at least one miniaturized version of said clock buffer is a scaled down version of said clock buffer, said miniaturized version of said clock buffer having a scaling factor of K, said scaling factor

representing a number of said miniaturized clock buffers utilized to minimize negative variations experienced by said clock buffer; and

means for minimizing negative variations experienced by said clock buffer.

16. (Original) The system of claim 15, wherein said receive logic is situated on an application specific integrated circuit.

17. (Original) The system of claim 15, wherein said negative variations are selected from the group consisting of process, voltage and temperature.

18. (Original) The system of claim 15, wherein said clock buffer is capable of driving a received clock signal to a register located within said receive logic.

19. (Previously Presented) The system of claim 18, wherein a setup time of said receive logic is represented by the equation:

$$T_{setup} = T_{reg\text{-}sctup} + 1.1 \times (-T_{clk\text{-}dly}) - T_{clk\text{-}rte}(min)$$

wherein, $T_{reg\text{-}setup}$ is a setup time for said register, $T_{clk\text{-}dly}$ is a delay contributed by said clock buffer, and $T_{clk\text{-}rte}(min)$ is a minimum delay contributed by propagation of said clock signal to said register.

20. (Previously Presented) The system of claim 18, wherein a hold time of said receive logic is represented by the equation:

$$T_{hold} = T_{reg\text{-}hold} + 1.1 \times (T_{clk\text{-}dly}) + T_{clk\text{-}rte}(max)$$

wherein, $T_{reg\text{-}hold}$ is a hold time for said register, $T_{clk\text{-}dly}$ is a delay contributed by said clock buffer, and $T_{clk\text{-}rte}(max)$ is a maximum delay contributed by propagation of said clock signal to said register.

21. (Currently Amended) A system comprising:

a register having a clock input and a data input;

a clock receiver for receiving a clock signal;

at least one clock buffer for driving the clock signal to the register;

a data receiver for receiving a data signal; and

at least one data delay device;

wherein the at least one data delay device is configured to substantially match the delay of the clock signal from the clock receiver to the clock input of the register with the delay of the data signal from the data receiver to the data input of the register; and

wherein each of the at least one data delay device is a scaled down version of the at least one clock buffer with respect to size, power, and load.

22. (Previously Presented) The system of claim 21, wherein the at least one data delay device is configured to mimic the delay of the at least one clock buffer.

23. (Previously Presented) The system of claim 21, wherein the number of the at least one data delay device is equal to the number of the at least one clock buffer.

24. (Canceled)

25. (Previously Presented) The system of claim 21, wherein the delay of the at least one clock buffer is subject to variations, and the at least one data delay device is configured to duplicate the variations.

26. (Previously Presented) The system of claim 21, further comprising a setup time represented by the equation:

$$T_{setup} = T_{reg\text{-}setup} + 1.1 \times (-T_{clk\text{-}dly}) - T_{clk\text{-}rte}(min)$$

wherein, $T_{reg\text{-}setup}$ is a setup time for the register, $T_{clk\text{-}dly}$ is a delay contributed by the at least one clock buffer, and $T_{clk\text{-}rte}(min)$ is a minimum delay contributed by propagation of the clock signal to the register.

27. (Previously Presented) The system of claim 21, further comprising a hold time represented by the equation:

$$T_{hold} = T_{reg\text{-}hold} + 1.1 \times (T_{clk\text{-}dly}) + T_{clk\text{-}rte}(max)$$

wherein, $T_{reg\text{-}hold}$ is a hold time for the register, $T_{clk\text{-}dly}$ is a delay contributed by the at least one clock buffer, and $T_{clk\text{-}rte}(max)$ is a maximum delay contributed by propagation of the clock signal to the register.